

FIG. 1

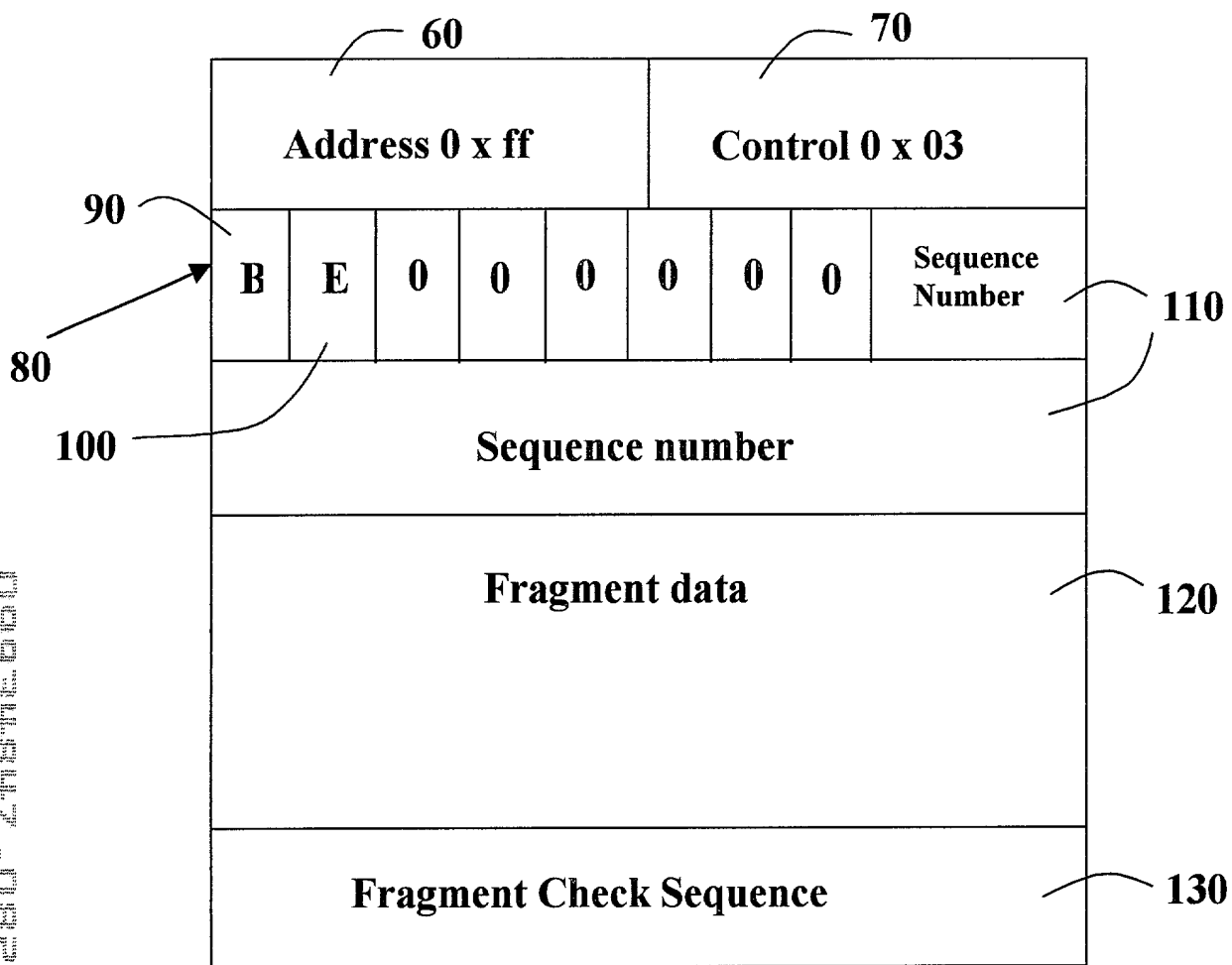


FIG. 2

Standard HDLC Frame

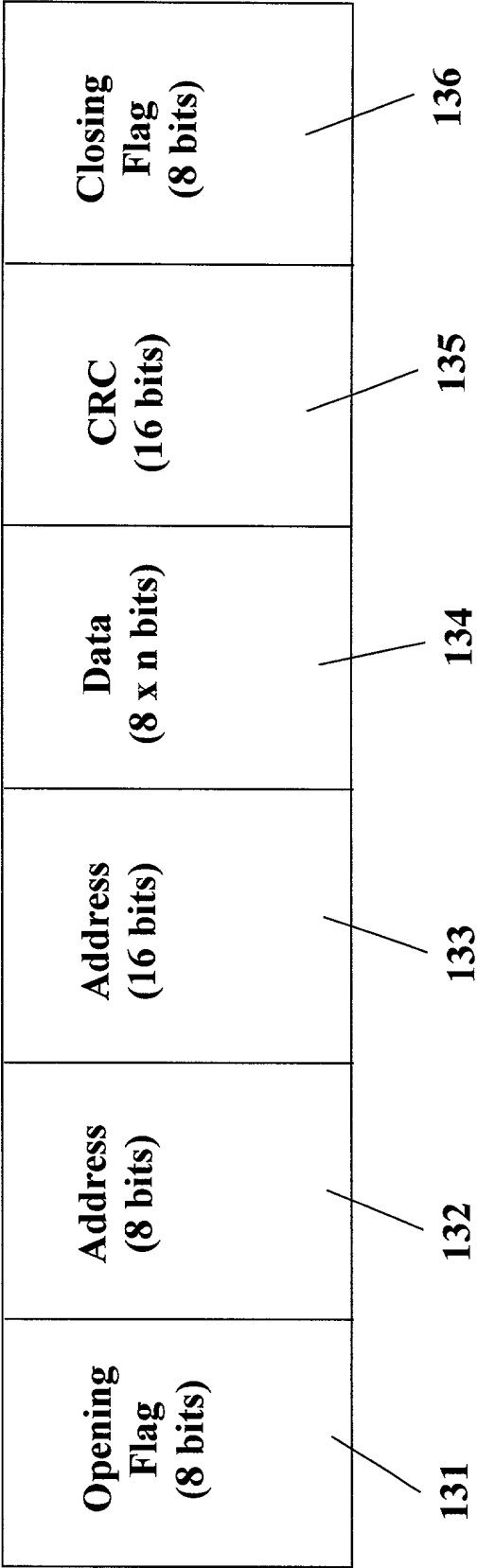


FIG. 2A

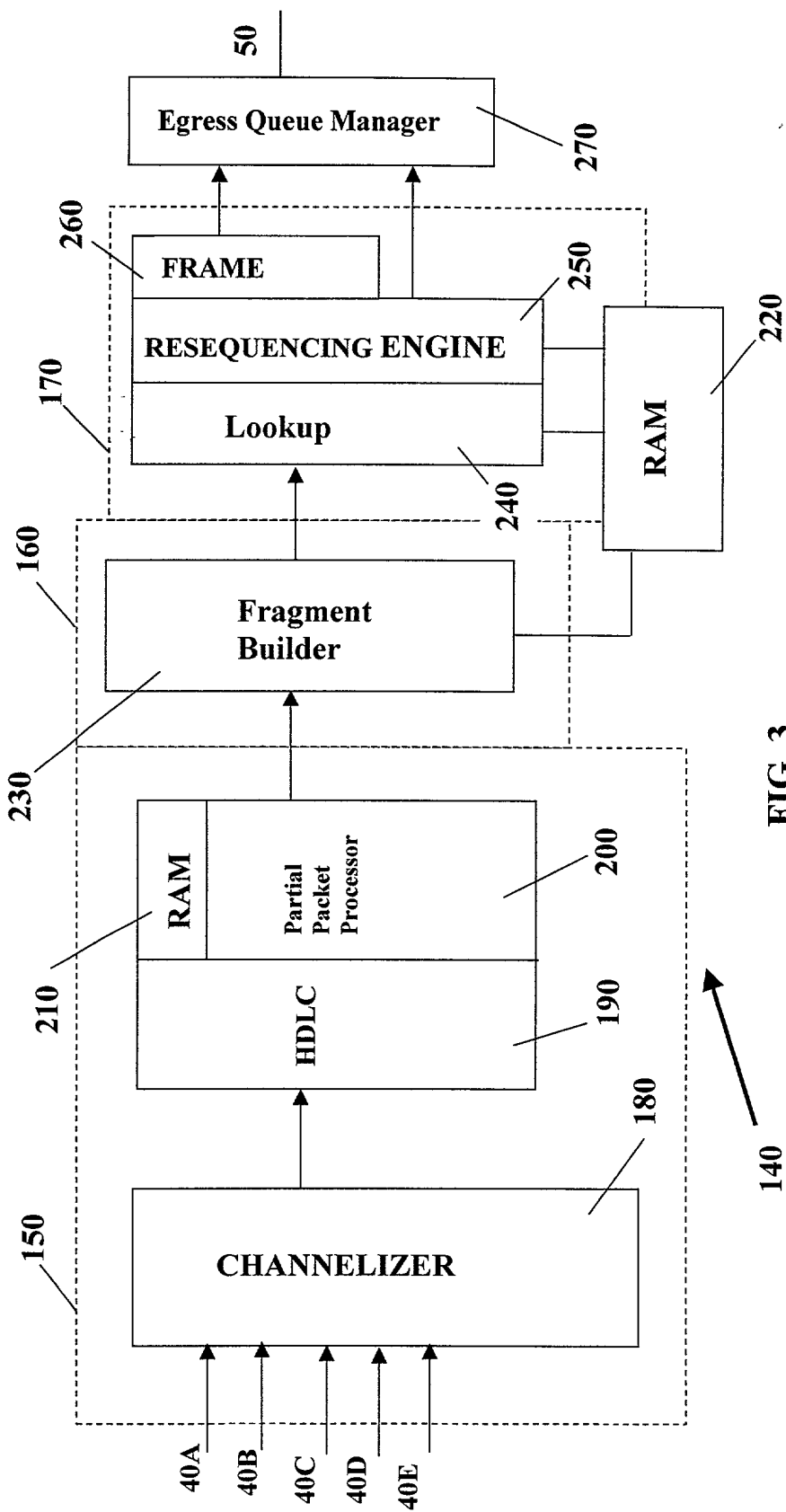


FIG. 3

Ptr Address	Memory Address	Next Ptr
A	000	B
B	031	C
C	063	D
D	095	NULL(END)
E	127	G
F	159	UNUSED
G	191	J
H	223	I
I	255	NULL
J	287	K
K	319	NULL

FIG. 4

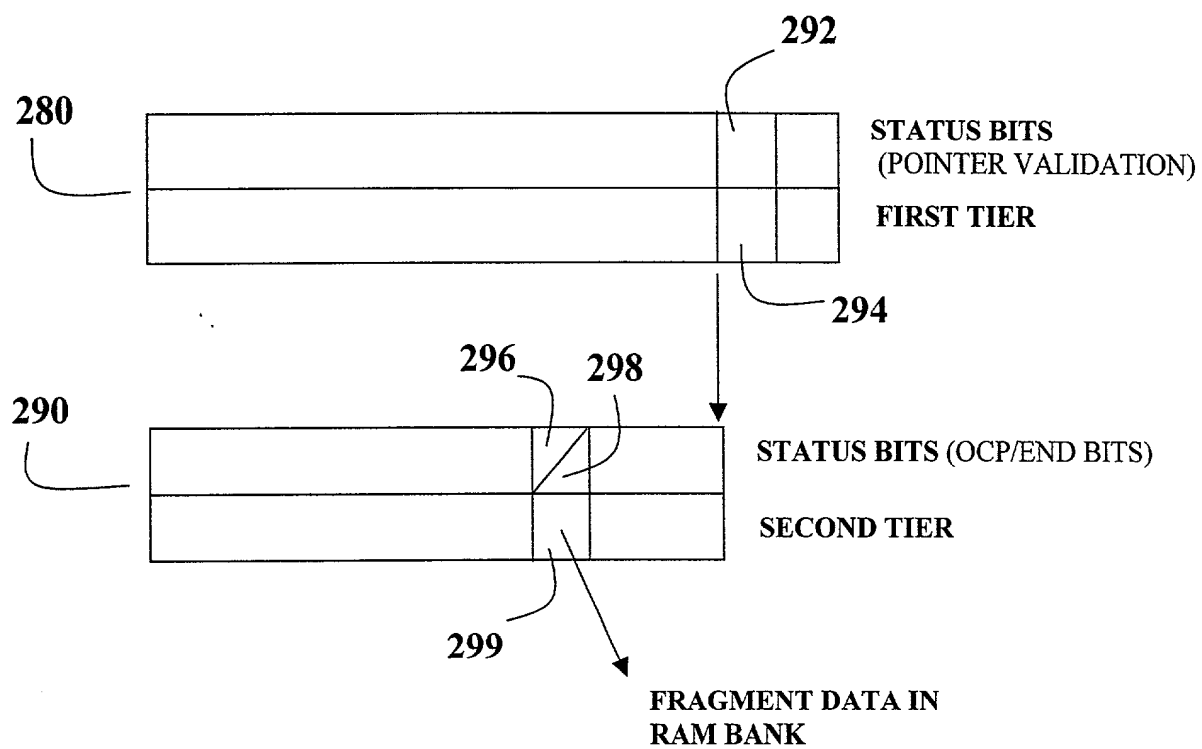


FIG. 5

X + 5				
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X + 5			X + 2	
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X + 5	X + 4		X + 2	
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X + 5	X + 4	X + 3	X + 2	
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X + 5	X + 4	X + 3	X + 2	X + 1
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FIG. 6

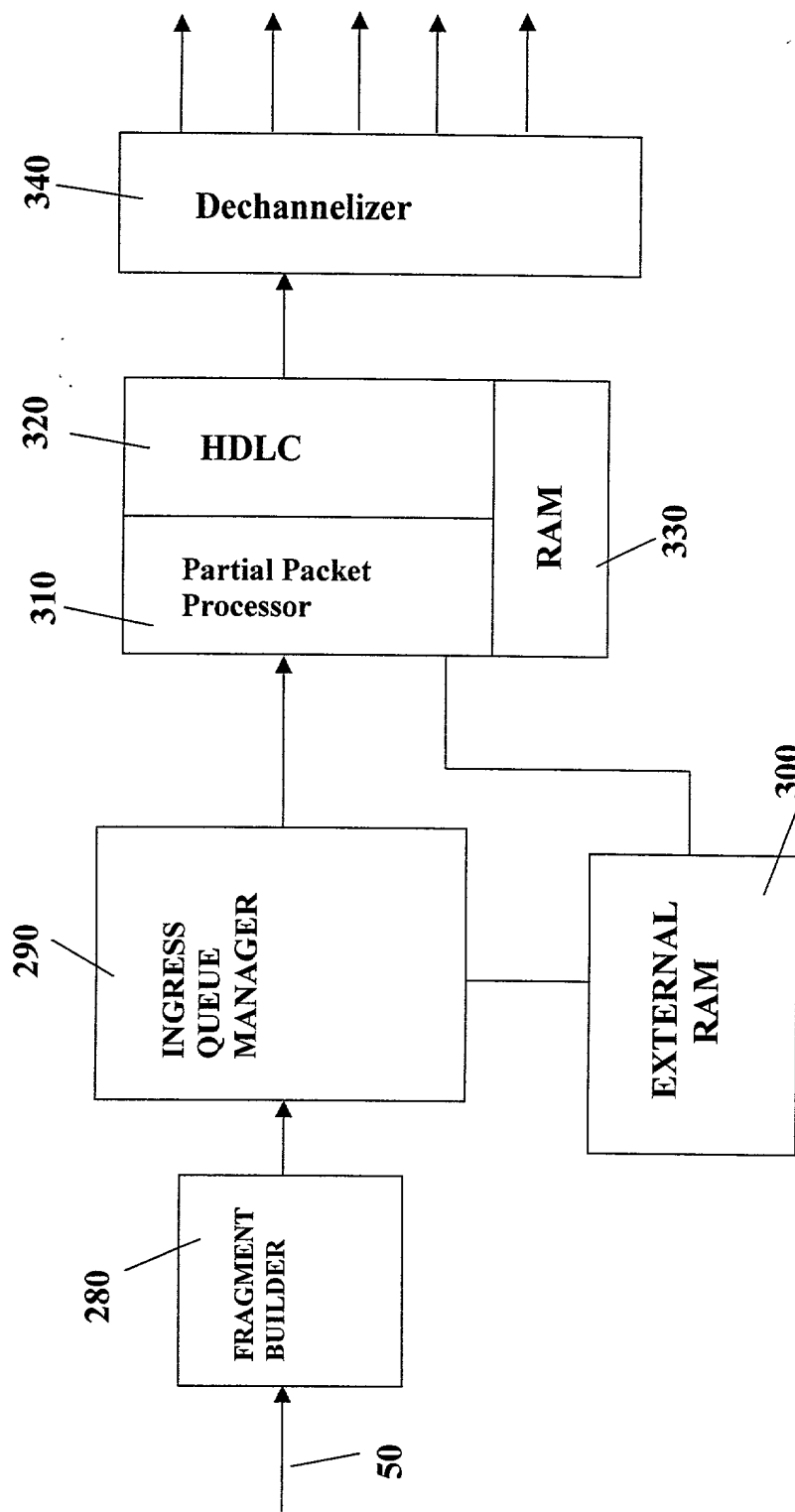


FIG. 7

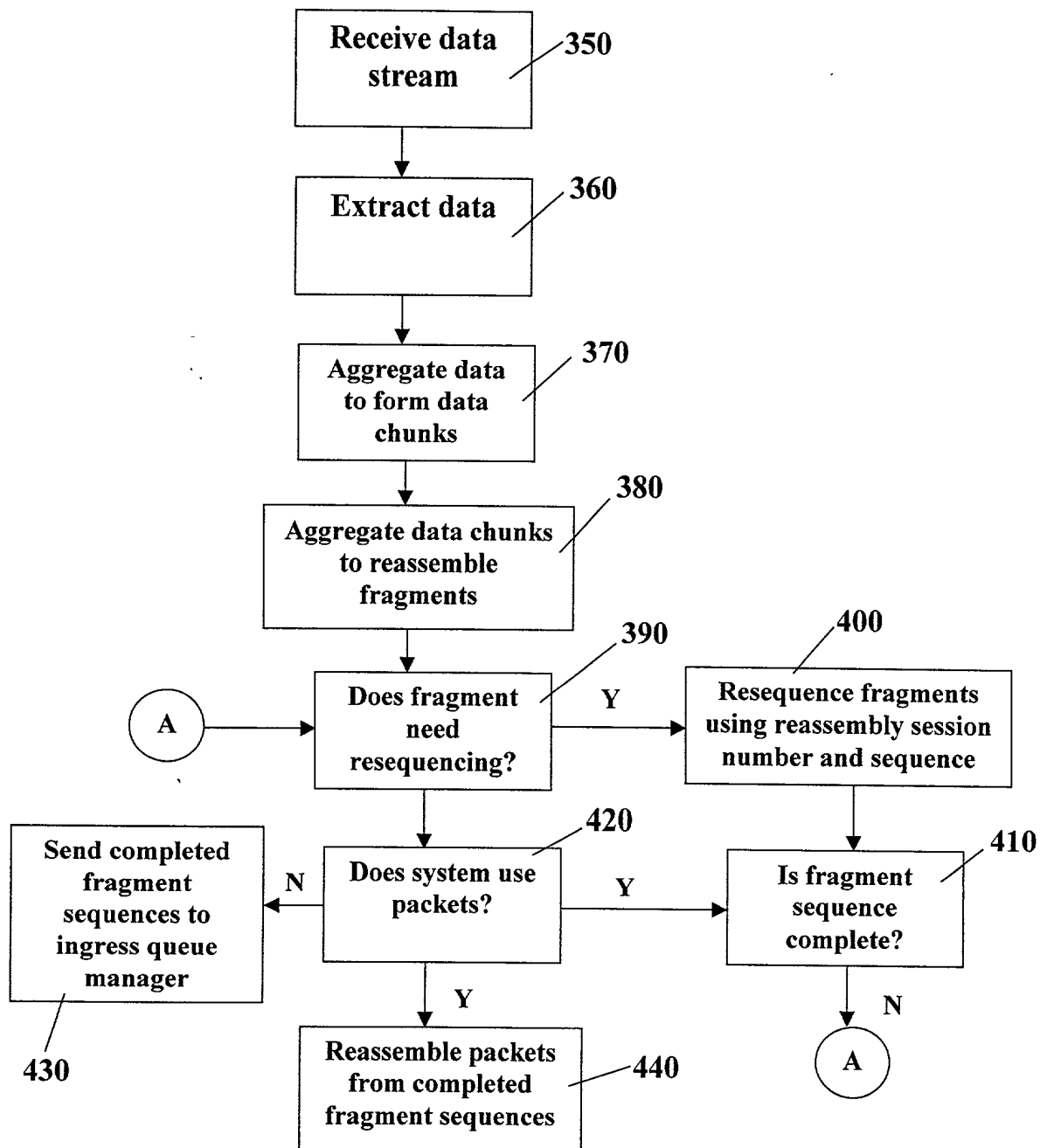


FIG. 8

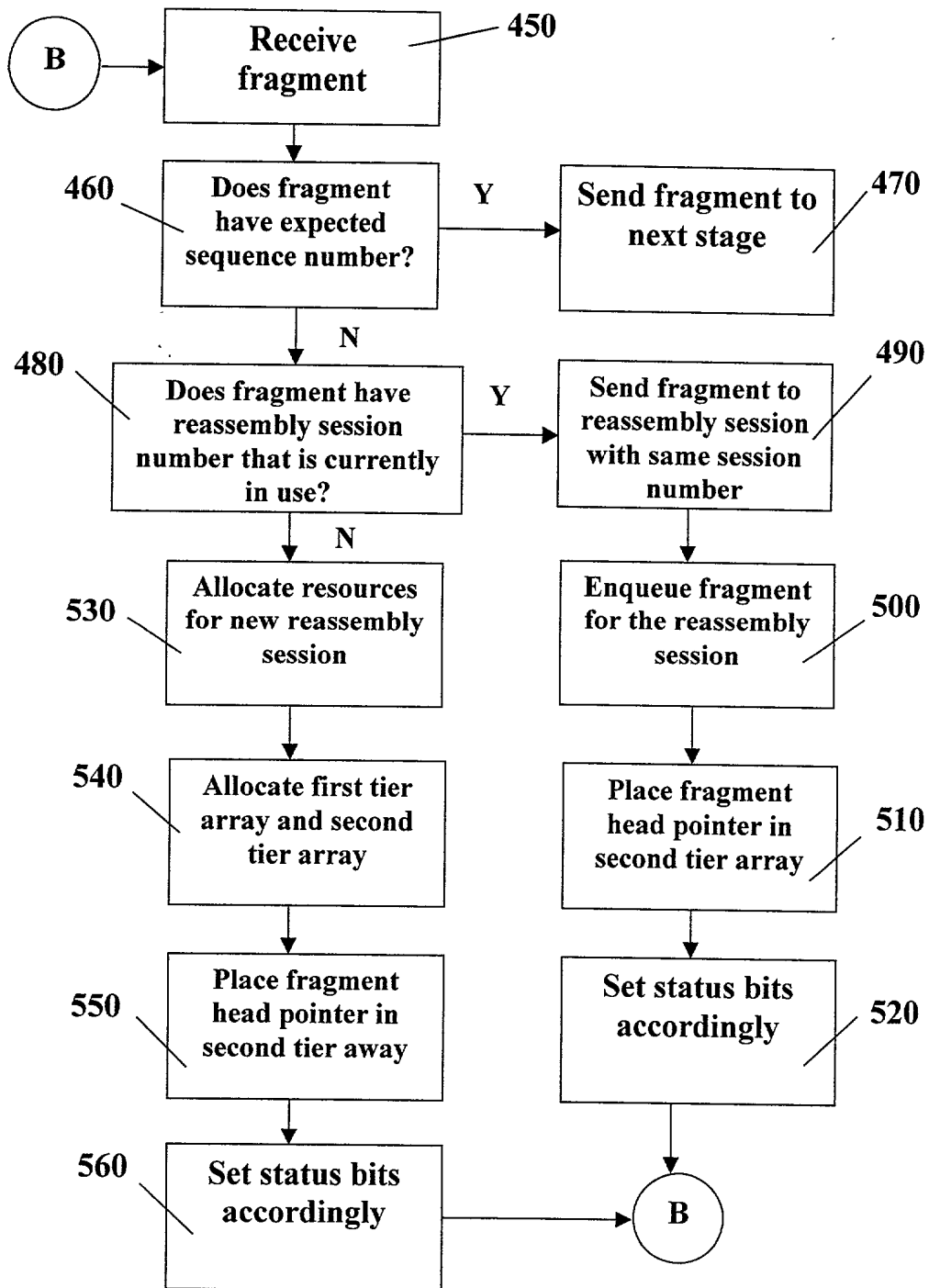


FIG. 9

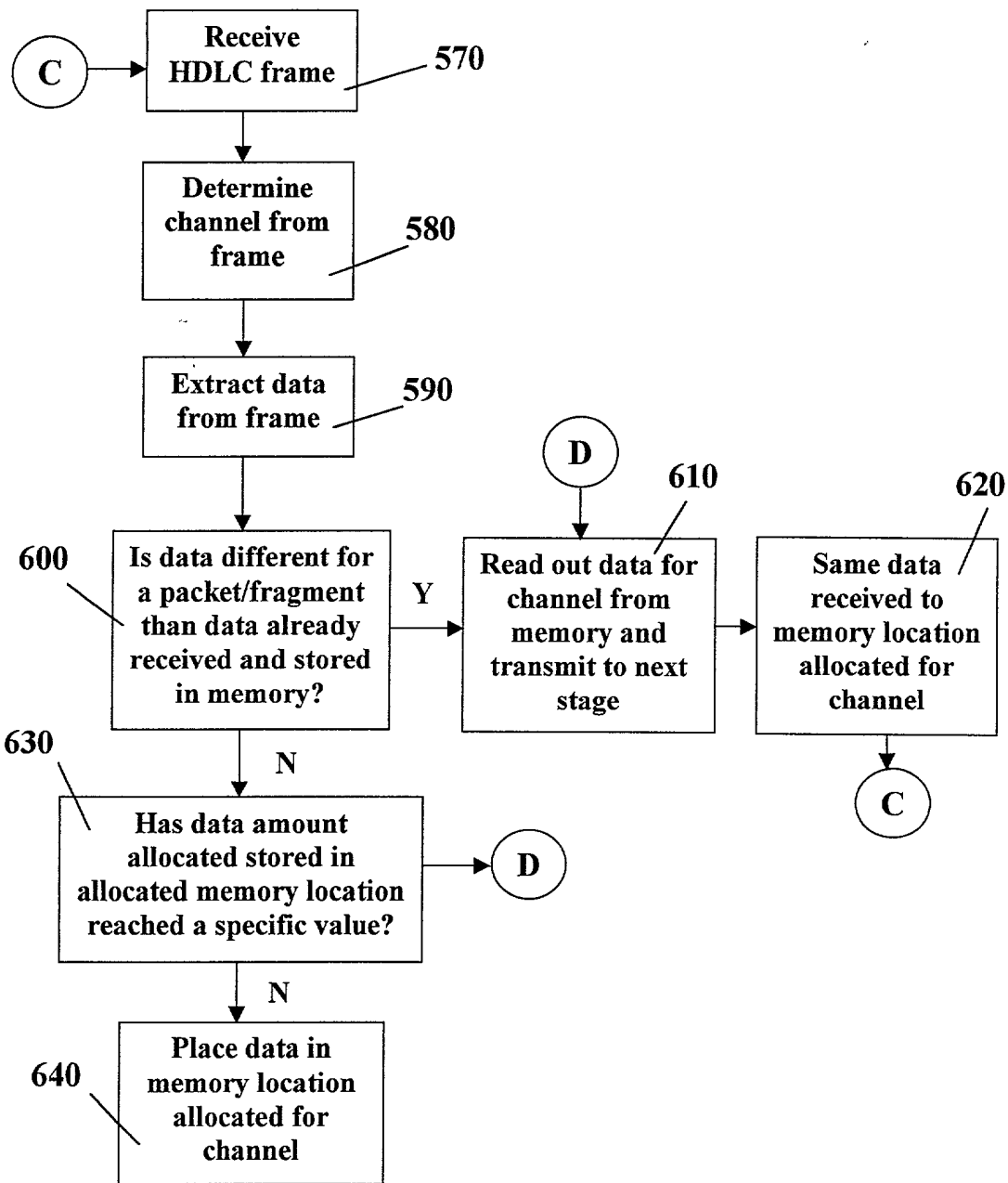


FIG. 10

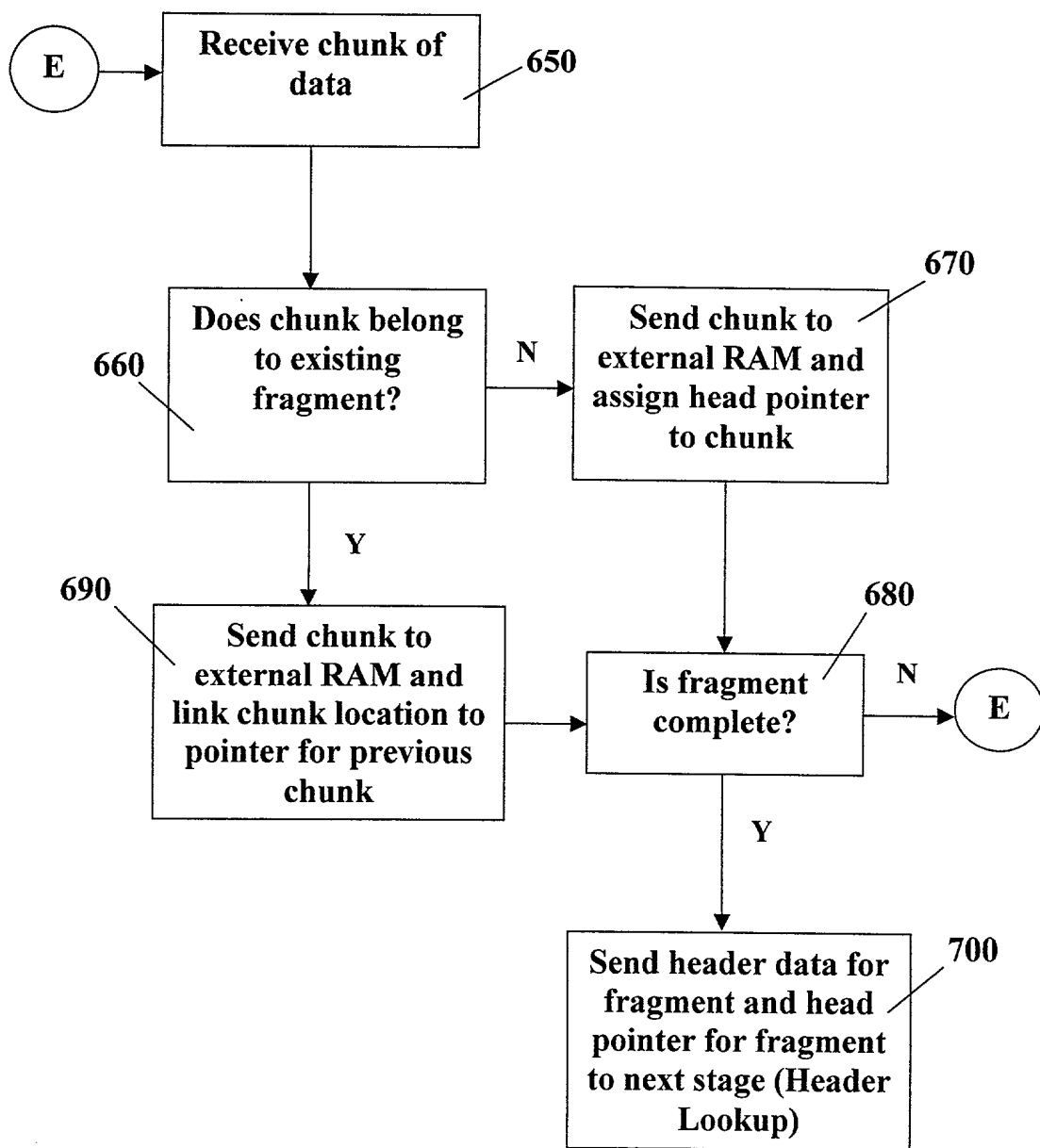


FIG. 11